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GB 2254486 A	GB 2174535 A	EP 0476975 A
EP 0413482 A	EP 0413481 A	EP 0405262 A
EP 0107217 A	WO 92/20087 A	US 4780395 A
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UK CL (Edition M) H1D DABXA DAB6 DAC4 DAF10 DBT1 DJ DPB DPD
INT CL[5] H01J
Online databases:WPI

(54) **Electron multiplier, e.g. for a field emission display**

(57) An electron multiplier comprises first and second perforate laminar electrodes (370, 380). An electrically non-conductive layer (310), e.g. of aluminium oxide, separates the electrodes. The layer defines channels (330) between perforations of the first electrode and perforations of the second electrode. The channels are lined with an electrically resistive layer (350), e.g. tin oxide, and an electron emissive layer (360), e.g. comprising lead, overlying the electrically resistive layer. The electron multiplier is especially useful for amplifying electron beam current in a field emission display, the channels (330) being aligned with an array of electron emissive tips.

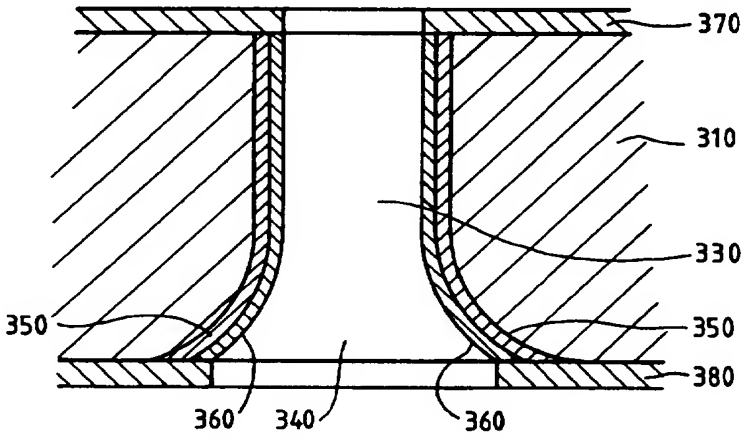

FIG. 4

GB 2 293 042 A

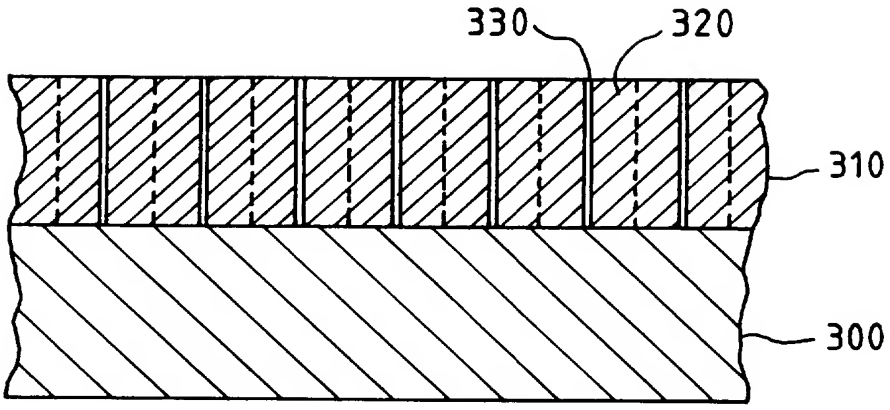

FIG. 1

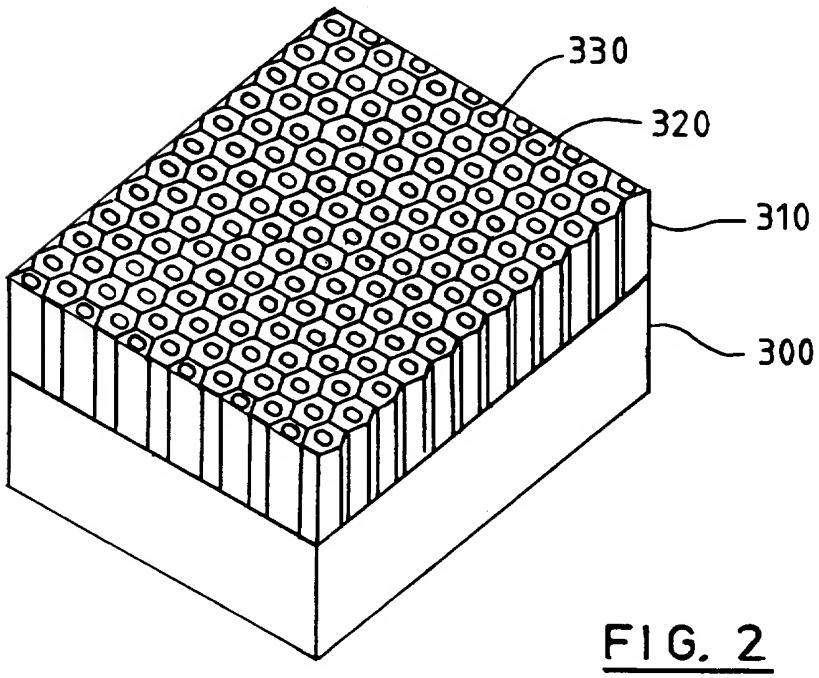

FIG. 2

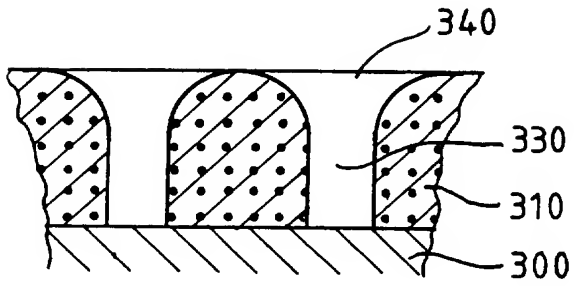

FIG. 3

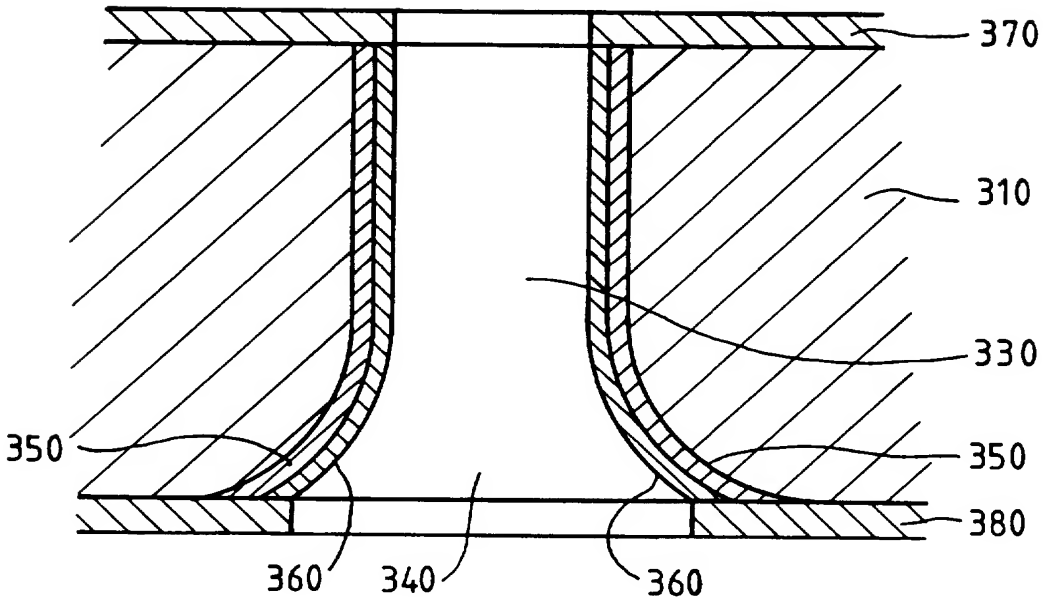

FIG. 4

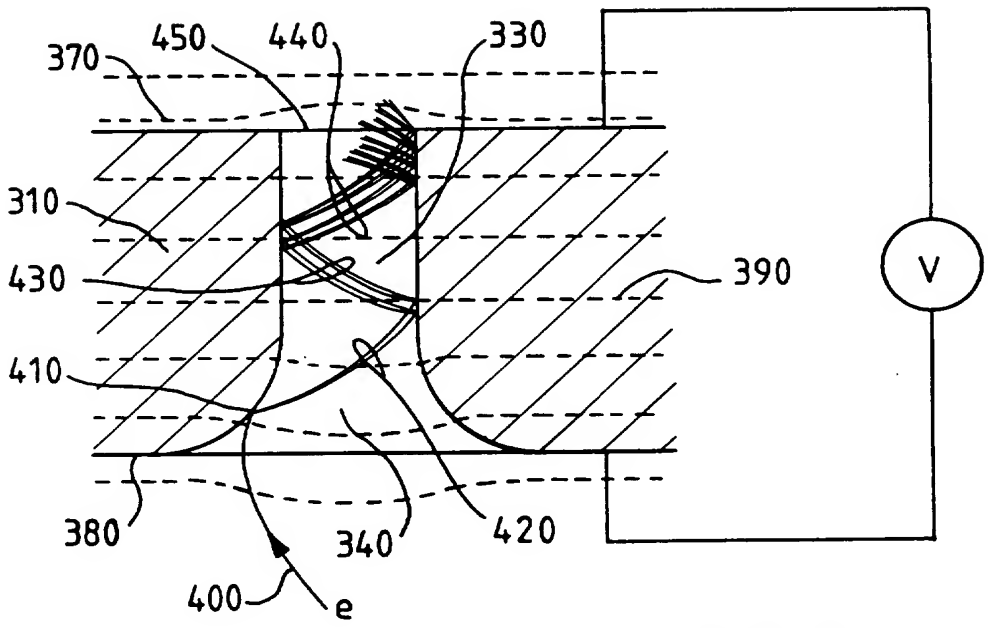
370
450
440
330
310
430
390
V
410
380
340
420
400
e

FIG. 5

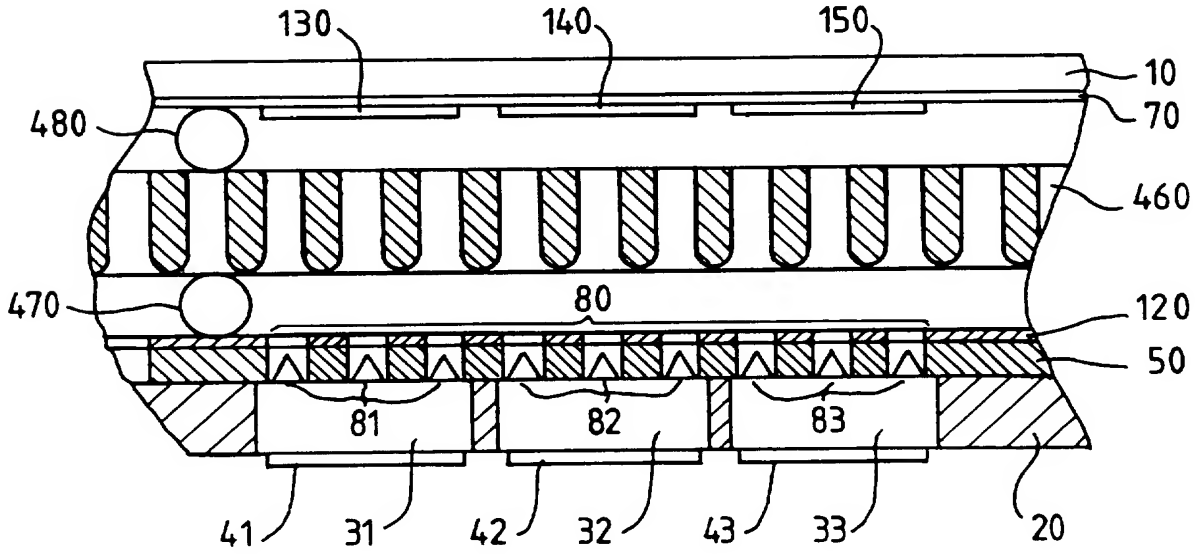
130
140
150
10
480
70
460
470
80
120
50
81
82
83
41
31
42
32
43
33
20

FIG. 6

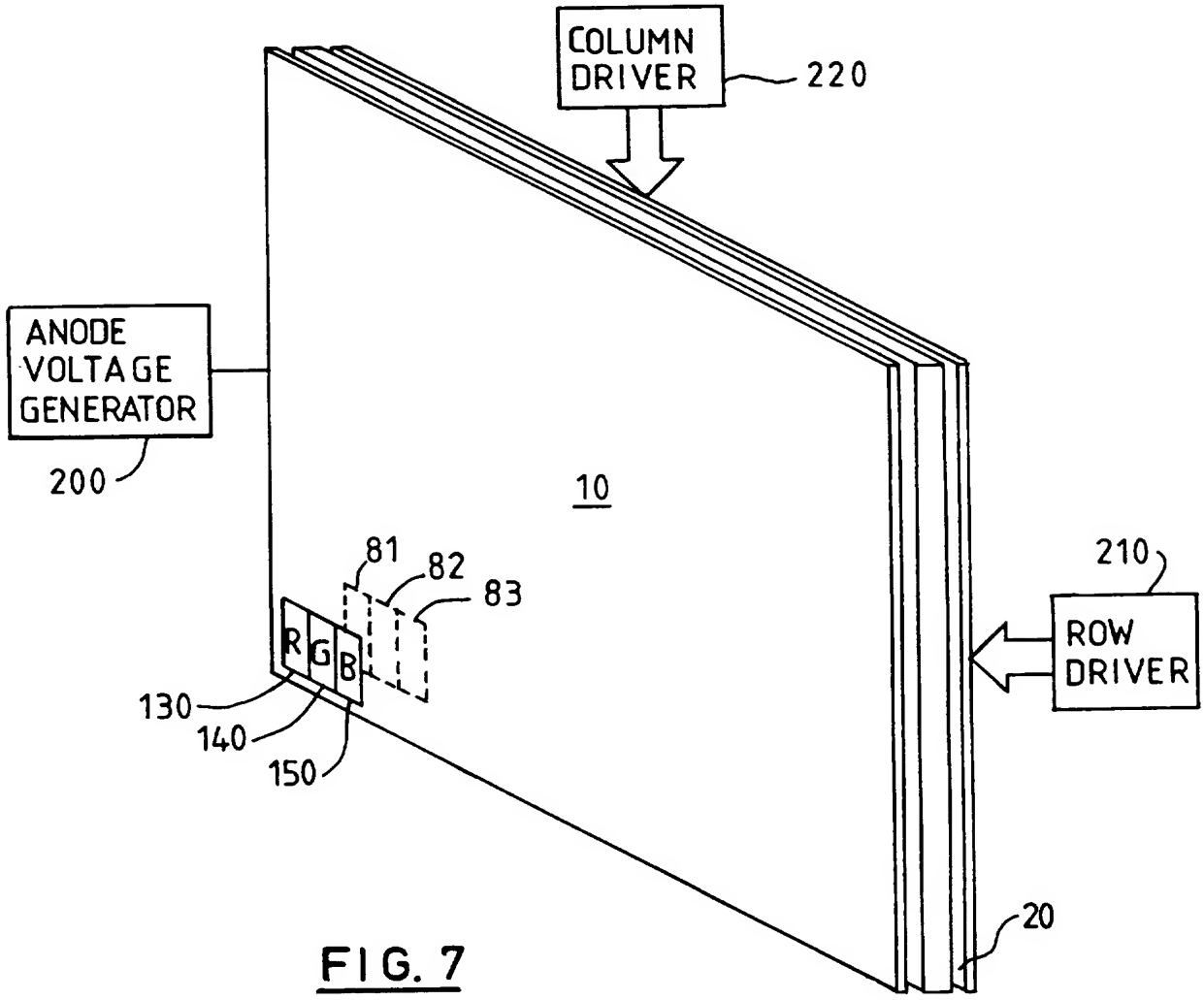
COLUMN DRIVER
220
ANODE VOLTAGE GENERATOR
200
10
81
82
83
R
G
B
130
140
150
210
ROW DRIVER
20

FIG. 7

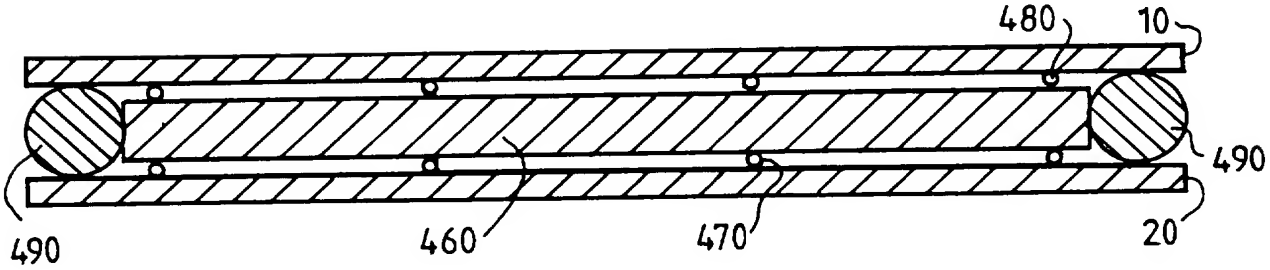
480
10
490
490
460
470
20

FIG. 8

ELECTRON MULTIPLIERS

The present invention relates in general to electron multipliers and to channel plate electron multipliers in particular.

A typical channel plate electron multiplier comprises a stack of alternately arranged perforate laminar electrodes or dynodes and perforate laminar non-conductive separators aligned to form electron multiplier channels. In operation, a potential difference is maintained across the electrode/separator stack. Primary electrons are released into the channels from one or more cathodes on one side of the stack. In the channels, the primary electrons are accelerated towards the other side of the stack under the influence of the potential difference between the electrodes. As they pass through the channels, the primary electrons impact electrodes in the channels. Each impact generates a secondary emission of a greater number of electrons. These are in turn accelerated through the stack under the influence of the potential difference. As they pass through the channels, the secondary electrons impact the successive electrodes generating still further electron emissions. The density of electrons emerging from the stack in thus higher than the density entering the stack. The multiplier thus amplifies the input current by secondary emission of electrons.

Channel plate electron multipliers of the kind described above are typically produced by the following process. First, a bundle a glass tubes are drawn out. This reduces the diameter of the tubes and fuses them together. Drawn bundles are then grouped into secondary bundles and the drawing step repeated. The drawing and grouping steps are successively repeated until desired tube and bundle dimensions are obtained. The finished bundle is then sliced into plates. The opposing surfaces of each plate are polished. The polished surfaces are then alternately stacked with electrodes to form the multiplier. Another method of forming a channel plate multiplier is described in GB 2 023 333. In practise, these processes are expensive because they have many labour intensive and time-consuming process steps.

In accordance with the present invention, there is now provided an electron multiplier comprising: first and second perforate laminar electrodes; an electrically non-conductive layer separating the electrodes, the layer defining channels between perforations of the first

electrode and perforations of the second electrode; characterised in that the channels are lined with an electrically resistive layer and an electron emissive layer overlying the electrically resistive layer.

This advantageously provides an electron multiplier that is easier and therefore cheaper to produce than conventional electron multiplier designs.

The non-conductive layer preferably comprises crystalline aluminium oxide. A layer of Crystalline aluminium oxide can be conveniently produced by anodising an aluminium sheet.

In a preferred embodiment of the present invention, the channels are the pores in the crystal structure of the aluminium oxide layer. The pores in the crystal structure of the aluminium oxide layer extend perpendicular to the surface of layer. The pores are less than 1 um in diameter and spaced from each other by distance of approximately 5 um. Because, in accordance with the present invention, the pores in the crystal structure of the aluminium oxide define the channels of the multiplier, conventional channel forming process steps, such as photo-chemical etching for example, are not required. Furthermore, the relatively narrow, closely packed channels are especially useful where the electron sources closely packed. As will be described later, this embodiment of the present invention is particularly applicable to field emission display technology in which the electron sources are electron emissive tips spaced from each other by typically 5 um and each having a diameter typically in the range 1 to 2 um. The present invention is also applicable to flat cathode ray display tubes where electron beams are deflected through angles approaching 180 degrees.

In this and other embodiments of the present invention, the ends of the channels are flared on at least one side of the non-conductive layer. This advantageously increases the electron capture cross section of the channels in the multiplier.

The electron emissive layer preferably comprises lead which can conveniently be deposited by hydrolysis of a lead salt, for example. Similarly, the electrically resistive layer comprises tin oxide which can conveniently be also deposited via hydrolysis, this time of a tin salt.

Viewing the present invention from another aspect, there is now provided a method of making an electron multiplier comprising: forming an electrically non-conductive layer having channels defined therein; forming an electrically resistive layer in the channels; forming an electron emissive layer on the resistive layer; separating first and second perforate laminar electrodes with the non-conductive layer; and, aligning the channels with perforations of the first and second electrode.

As mentioned earlier, the electron multiplier of the present invention is particulary applicable to field emission display technology

US Patent 4,857,799 describes an example of a conventional colour field emission display. Such displays typically include a phosphor coated screen overlying and spaced from a two dimensional matrix of field emission cathodes. US Patents 3,789,471, 3,665,241, and 3,775,704 describe examples of, and methods of producing such cathodes. Each cathode includes three arrays of electron emissive tips. Each array covers a surface area of typically 300 X 300 um. The arrays each comprise substantially the same number of tips (typically 1000). The screen is divided into pixels. Each pixel is divided into three sub-pixels. Each sub-pixel is formed by a phosphor corresponding to a different one of the primary colours Red, Green, and Blue. Each array in the cathode faces a different sub-pixel of a corresponding pixel. The arrays are individually addressable via row and column conductors.

In operation, voltages determined by input red, green, and blue video signal are sequentially applied to the row and column conductors to address each cathode in turn in a raster pattern. The voltages interact to generate a high localised electric field at each tip. The localised field causes electrons to be emitted from the tips. A potential difference, which is typically in the range of 300 to 400V, is maintained between the matrix and the screen. The electrons are accelerated from the tips towards phosphors on the screen by the electric field between the screen and the matrix. The phosphors are excited by incident electrons to display an image on the screen as a function of the input video signal.

The phosphors typically operate at relatively high electron beam currents and at relatively low voltages compared with conventional high voltage scanned cathode ray display tubes. At low voltage, the electron

energy is dissipated only at the surface layers of the phosphor. This can lead to electron beam damage, which, in turn, may produce volatile decomposition products leading to a loss in emission efficiency. The emission tips operate at between 1 and 10 per cent of their maximum current ratings, and are long-lived. However, the emission efficiency depends super-exponentially on the work function of the tip material. A slight decomposition of the phosphor might not itself present a problem. However, if the work function of the tips is changed by absorption of the decomposition products into the tips, emission efficiency may be severely degraded. Operating the field emission display at phosphors voltages of 300 to 400V requires the matrix and the screen to be held at a separation of 100 to 150 um. This requires spacers with aspect ratios of up to 10:1 if the spacers are not to be visible. Conventionally, the tips of the display require a "select" voltage of 80V and a "non-select" voltage of 50V. This adds significantly to driver circuitry cost and to power consumption in the addressing circuitry.

Viewing the present invention from another aspect, there is provided a field emission display comprising: a screen; a back-plate carrying an array of electron emissive tips directed towards the screen; and an electron multiplier between the back-plate and screen, the channels of the electron multiplier being aligned with the tips on the back-plate.

The electron multiplier amplifies the electron beam currents from the tips, thereby permitting the beam currents drawn from the tips to be reduced. The tips can therefore be operated at much lower voltages than conventional field emission displays. This allows the operating voltages of driver circuitry associated with the field emission display to be significantly reduced.

In conventional field emission displays, spacers separate the back plate from the screen by a distance of typically 100 um. This distance has been found sufficient to sustain an anode voltage of between 300 and 400 V. Because, in accordance with the present invention, the electron multiplier positioned between the screen and the back plate, much higher anode voltages can be sustained in the field emission display of the present invention. This advantageously permits higher voltage phosphors to be used. In general, higher voltage phosphors, such as phosphors which

normally operate at 1000V for example, are more stable and more widely available than phosphors which operate at 300 to 400V.

Furthermore, the electron multiplier in the field emission display of the present invention provides a physical barrier between the tips on the back-plate and the phosphor on the screen. This reduces any emitter degradation which might other wise occur due to phosphor degradation.

Also, because the electron multiplier is positioned between the back-plate and the screen, smaller, less obtrusive spacers can be used to separate the back-plate and screen from the multiplier.

Preferably, the multiplier comprises: first and second perforate laminar electrodes; an electrically non-conductive layer separating the electrodes, the layer defining the channels of the multiplier between perforations of the first electrode and perforations of the second electrode; characterised in that the channels are lined with an electrically resistive layer and an electron emissive layer overlying the electrically resistive layer.

In preferred embodiments of a display of the present invention, the non-conductive layer comprises crystalline aluminium oxide. The channels may then be conveniently provided by the pores in the crystal structure of the aluminium oxide layer.

The ends of the channels are preferably flared on at least one side of the non-conductive layer. Advantageously, the ends of the channels closest to the tips may be flared to improve electron capture from the tips.

The electron emissive layer may comprise lead and the electrically resistive layer may comprise tin oxide.

It will be appreciated that the present invention extends to a method of making a field emission display comprising: forming an array of electron emissive tips on a back plate; directing the tips formed on the back-plate towards a screen; positioning an electron multiplier of the kind described in paragraph four above. between the back plate and the screen; and, aligning the channels of the electron multiplier with the tips on the back plate.

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a perspective view of an anodised aluminium sheet;

Figure 2 is a cross-sectional view of the sheet;

Figure 3 is a cross-sectional view of the sheet after etching;

Figure 4 is a cross-sectional view of a channel plate electron multiplier of the present invention;

Figure 5 is a cross-sectional view of the multiplier of the present invention in operation;

Figure 6 is a magnified cross-sectional view of a field emission display of the present invention;

Figure 7 is a perspective view of a field emission display of the present invention; and

Figure 8 is a cross-sectional view of a field emission display of the present invention.

What follows is a description of a process for fabricating a channel plate electron multiplier of the present invention.

With reference to Figures 1 and 2, a sheet of aluminium 300 is anodised to produce an aluminium oxide layer 310 to a thickness typically between 0.5 to 1.0 mm. Layer 310 has a crystal structure resembling an array of upstanding hexagonal extrusions 320. Each extrusion 320 is typically around 5um wide. Passing through the centre of each hexagonal extrusion 320 is a pore 330 of less than 1 um diameter communicating between opposite surfaces of the oxide layer 310.

Referring now to Figure 3, the openings 340 to the pores 330 are enlarged by immersing the anodised sheet in an etch bath containing an etchant for partially dissolving the oxide layer 310. The etching process is halted by chemical neutralisation of the etchant and rinsing.

Referring to Figure 4, the remaining aluminium 300 is now etched from the rear surface of the oxide layer to leave a free standing sheet 310 of porous aluminium oxide. A partially conducting layer 350 is now formed on all surfaces of the sheet. Layer 350 may be formed by the following technique. Initially, the sheet 310 is dried at around 100 degrees centigrade. The dried sheet 310 is then immersed in a dilute solution of tin chloride in hydrochloric acid. Excess solution is removed and the sheet 310 is heated rapidly to about 350 degrees centigrade, at which temperature the tin chloride hydrolyses to form an absorbed layer 350 of conducting tin oxide. An electron emissive layer 360 is now formed on layer 350. Layer 360 may be constituted by a lead-rich layer for example. Layer 360 may be formed via a process similar to that used to form layer 350, with the tin salt replaced by a lead salt such as lead silicate, for example. It will be appreciated that in other embodiments of the present invention, the partially conducting layer 350 and the electron emissive layers may be formed by different processes to those hereinbefore described. Upper and lower electrodes 370 and 380 of an electrically conductive material such as niobium for example, are then deposited on the upper and lower surfaces of the sheet 310.

Referring now to Figure 5, in operation, a voltage V is maintained across the across sheet 310 by a voltage source V connected to upper and lower electrodes 370 and 380. A primary electron e from an electron source (not shown) enters one of channels 330 through enlarged entrance 340 and impacts the wall of the channel at 410. The impact of the primary electron with layer 360 causes a secondary emission of a second electron. The voltage across electrodes 370 and 380 sets up a potential gradient along the length of the channel via partially conducting layer 350. The corresponding electric field in the channel, illustrated in Figure 5 by field lines 390 accelerates the primary and secondary electrons, shown at 420, towards the exit 450 from the channel 330. The primary and second electrons collide with layer 360 again each generating a further secondary electron emissions so that, at 430, there are 4 electrons generated by the original single electron stimulation. At 440, after a subsequent collision with layer 360, the four electrons have become eight. A further collision doubles the eight electrons at 440 to produce sixteen electrons at the exit 450 from the channel 370.

Because the openings 340 to the channels 330 are enlarged, the electron capture cross section of the multiplier is increased. This

advantageously improves the sensitivity the multiplier. It will be appreciated that the number of collisions, and thus the number of electron emissions, may be varied by varying the voltage between the electrodes to vary the gain of the multiplier.

Referring now to Figures 6, 7 and 8, a colour field emission display of the present invention comprises a transparent screen 10 superimposed and spaced from a back-plate 20 of an electrically non-conductive material such as Silicon Dioxide. The surface of the screen 10 facing the back-plate 20 carries a transparent layer 70 of an electrically conductive material such as Indium Tin Oxide. A matrix of cathodes 80 is provided on the surface of the back-plate 20 facing the face plate 10. Each cathode 80 comprises three arrays 81,82,83 of field emitter tips 81,82,83. The tips may be formed from Molybdenum. The arrays each occupy substantially equal areas. Each array corresponds to a different one of the three primary colours, Red, Green, and Blue. The tips are in the region of 1.4um diameter at a spacing of around 5um. The area of each array is typically 1250 square um.

The arrays 81,82,83 are each provided with an electrically conductive base 31,32,33 of, for example, amorphous silicon. Bases 31,32,33 extend through the back-plate 20. The bases 31,32,33 of the arrays of the cathodes in each column of the matrix are interconnected by electrically conductive strips or column conductors 41,42,43 of, for example, Niobium. The tips project towards the face plate 10 from pits formed in an insulator layer 50 of, for example, Silicon Dioxide. An electrically conductive gate layer 120, of, for example, Niobium is carried on the surface of the insulator layer 50 facing the screen 10. The gate layer 120 is common to each of the arrays 81,82,83 in each cathode. The gate layer 120 along each row of cathodes of the matrix array is connected to form a conductive strip or row conductor 120. Each array 81,82,83 of each cathode 80 of the display therefore can be addressed by orthogonal address lines in the form of the column conductors 41,42,43 connected to the bases 31,32,33 of the cathode 80 and the row conductor 120 perforated by the pits in which the tips of the array 81,82,83 are located. Phosphor strips 130,140,150 corresponding to the three primary colours R,G and B are provided on the conductive layer 70. Each one of the strips 130,140,150 faces a different one of the arrays 81,82,83.

In accordance with the present invention, the field emission display includes a channel plate electron multiplier 460 of the kind hereinbefore described with reference to Figures 1 to 5. Multiplier 460 is disposed between back-plate 20 and screen 10. Ball spacers 470 separate back plate 20 from the lower surface of multiplier 460. Similarly, ball spacers 480 separate the upper surface of multiplier 460 from screen 10. Ball spacers 470 and 480 are equally sized and between 25 and 50 um diameter. Spacers 470 and 480 are made from a dielectric material such as glass. Screen 10 is frit-sealed at 490 to back-plate 20 and the spaces between screen 10, multiplier 460 and back-plate 20 are evacuated. Spacers 470 and 480 prevent any distortions of back-plate 20, screen 10 and multiplier 450 that may other wise be caused by the enclosed vacuum. Spacers 470 are positioned equidistantly, typically about 20mm, from each other. Typically, 100 spacers 470 are used in a 26 cm display panel. Spacers 480 are distributed in a similar fashion. The number of spacers used is optimised as a function of the compressive strength of the spacer material and the thickness and elastic moduli of the materials used to form the screen 10, back-plate 20, and multiplier 450.

The back plate 20, conductors 40,120 and insulator layer 50 may be fabricated by conventional photolithography in combination with conventional processes such as planar diffusion, electrochemical etching, chemical vapour deposition or the like. The pits in which the tips are located may be ion etched into the insulator layer 50. The tips themselves may be fabricated by a combination of Electron Beam Evaporation and electrochemical etching. To mechanically strengthen the display, back-plate 20 may be fabricated on a glass substrate.

Conductive coating 70 is connected to an anode voltage generator 200, the column conductors are connected to a column driver 210, and the row conductors are connected to a row driver 220.

In operation, anode voltage generator 200 applies an anode voltage of around 400V to the conductive layer 70. Layer 70 will hereinafter referred to as the anode 70. Column driver 220 applies a drive voltage of around -15V to the row conductors 41,42,43. The drive voltage is transmitted to the tips in the arrays 81,82,83 via the bases 31,32,33. Row driver 210 applies a bias voltage of typically 15V to the row conductor 120 forming the gate layer. The voltages on the row and column

conductors cooperate in generating localised high electric fields. The localised fields cause electrons to be emitted from each tip. Electrode 380 of multiplier 460 is maintained at higher positive voltage than gate layer 120. Electrons from the tips are thus collectively accelerated by the resulting electric field towards openings 340 of multiplier 460. Electrode 370 is maintained at a higher voltage than electrode 380 but lower than the voltage on anode 70. Electrons from the tips are drawn up the channels 330 of multiplier 460 under the action of the potential difference between electrodes 380 and 370. In the channels 330, the electrons are multiplied by secondary emissions from the channel walls. At the exit from the channels the multiplied electrons are accelerated towards phosphors 130,140,150 by the high electric field between anode 70 and upper electrode 370. The phosphors 130,140,150 are excited by the incident electrons to generate the displayed image. Each cathode 80 corresponds a pixel of the displayed image. Each array of the cathode corresponds to one of the Red, Green and Blue sub-pixels of each pixel of the displayed image.

The row and column conductors are typically scanned by the drivers 210,220 to sequentially address drive and bias voltages to the arrays 81,82,83 of each cathode 80 in a raster fashion. The drive voltage on each cathode is maintained constant but the three gate voltages per cathode are varied as functions of Red, Green and Blue video signals respectively to produce the displayed image.

CLAIMS

1. An electron multiplier comprising: first and second perforate laminar electrodes (370,380); an electrically non-conductive layer (310) separating the electrodes, the layer defining channels (330) between perforations of the first electrode and perforations of the second electrode; characterised in that the channels are lined with an electrically resistive layer (350) and an electron emissive layer (360) overlying the electrically resistive layer.

2. An electron multiplier as claimed in claim 1, wherein the non-conductive layer comprises crystalline aluminium oxide.

3. An electron multiplier as claimed in claim 2, wherein the channels are the pores in the crystal structure of the aluminium oxide layer.

4. An electron multiplier as claimed in any preceding claim, wherein the ends of the channels are flared on at least one side of the non-conductive layer.

5. An electron multiplier as claimed in any preceding claim, wherein the electron emissive layer comprises lead.

6. An electron multiplier as claimed in any preceding claim, wherein the electrically resistive layer comprises tin oxide.

7. A field emission display comprising: a screen (10); a back-plate (20) carrying an array of electron emissive tips directed towards the screen; and an electron multiplier (450) between the back-plate and the screen, the electron multiplier having channels aligned with the tips on the back-plate.

8. A display as claimed in claim 7, wherein the multiplier (450) comprises: first and second perforate laminar electrodes (370,380); an electrically non-conductive layer (310) separating the electrodes, the layer defining the channels (330) of the multiplier between perforations of the first electrode and perforations of the second electrode; characterised in that the channels are lined with an electrically resistive layer (350) and an electron emissive layer (360) overlying the electrically resistive layer.

9. A display as claimed in claim 8, wherein the non-conductive layer comprises crystalline aluminium oxide.

10. A display as claimed in claim 9, wherein the channels are the pores in the crystal structure of the aluminium oxide layer.

11. A display as claimed in any of claims 8 to 10, wherein the ends of the channels are flared on at least one side of the non-conductive layer.

12. A display as claimed in claim 11, wherein the ends of the channels closest to the tips are flared.

13. A display as claimed in any of claims 8 to 12, wherein the electron emissive layer comprises lead.

14. A display as claimed in any of claims 8 to 13, wherein the electrically resistive layer comprises tin oxide.

15. A method of making an electron multiplier comprising:

forming an electrically non-conductive layer (310) having channels defined therein;

forming an electrically resistive layer (350) in the channels;

forming an electron emissive layer (360) as the resistive layer;

separating first and second perforate laminar electrodes (370,380) with the non-conductive layer (310); and,

aligning the channels (330) with perforations of the first and second electrode.

16. A method of making a field emission display comprising:

forming an array of electron emissive tips on a back plate (20);

directing the tips formed on the back-plate towards a screen (10);

positioning an electron multiplier (450) as claimed in any of claims 1 to 6 between the back plate and the screen; and,

aligning the channels of the electron multiplier with the tips on the back plate.

Patents Act 1977 **Examiner's report to the Comptroller under Section 17 — 19 —** **(The Search report)**	Application number GB 9417740.9
Relevant Technical Fields (i) UK Cl (Ed.M) H1D (DAB6, DABXA, DAC4, DAF10, DPB, DJ) (ii) Int Cl (Ed.5) H01J	Search Examiner M J DIXON Date of completion of Search 23 SEPTEMBER 1994
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE DATABASE: WPI	Documents considered relevant following a search in respect of Claims :- 1 TO 6, 15 AND 16

Categories of documents

X:	Document indicating lack of novelty or of inventive step.	**P:**	Document published on or after the declared priority date but before the filing date of the present application.
Y:	Document indicating lack of inventive step if combined with one or more other documents of the same category.	**E:**	Patent document published on or after, but with priority date earlier than, the filing date of the present application.
A:	Document indicating technological background and/or state of the art.	**&:**	Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	EP 0413482 A	(GALILEO) see especially Figure 9	1, 2, 15
X	EP 0413481 A	(GALILEO) see especially Figures 7 and 8	1, 2, 15
X	US 4780395 A	(TOSHIBA) see films 21 and 22	1, 5, 15

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

Patents Act 1977
Examiner's report to the Comptroller under Section 17
(The Search report) : Second Search

Application number
GB 9417740.9

Relevant Technical Fields

(i) UK Cl (Ed.N) H1D (DAB6, DABXA, DAF10, DBT1, DAC4, DPD)

(ii) Int Cl (Ed.6) H01J (3/02, 29/02, 29/48, 31/12)

Search Examiner
M J DIXON

Date of completion of Search
13 SEPTEMBER 1995

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE: WPI

Documents considered relevant following a search in respect of Claims :-
7-14

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	GB 2254486 A	(SONY) see especially Figure 6	7
X	GB 2174535 A	(PHILIPS) see especially page 2 line 12	7
X	WO 92/20087 A	(EASTMAN KODAK) see eg Figures 2 to 5	7
X	EP 0476975 A	(YEDA) the whole document	7
X	EP 0405262 A	(MATSUSHITA) see eg column 5, lines 19 to 33; column 9 line 48 et seq	7
X	EP 0107217 A	(PHILIPS) see especially page 5 lines 4 to 6	7
X	US 4577133 A	(WILSON) see the whole document	7

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).